GUJARAT UNIVERSITY

BE ATKT EXAM 2013

Branch: Computer Engineering/ IT Engineering **Semester: VII**

Subject: Elective - VLSI

1	Discuss VLSI Design Methodologies in brief.
2	Explain different physical components of threshold voltage. Also derive the equation for threshold voltage for n-channel device.
3	Discuss different device isolation techniques for MOS Transistor.
4	Discuss Layout Design Rules
5	Explain following terms: (i) Yield (ii) Manufacturability (iii) Standard Cell based Design
6	Explain Gradual Channel approximation for MOSFET Operation. Also derive the drain current equation.
7	Draw and explain input and output waveforms of typical inverter. Also explain Delay time definitions.
8	Explain design and analysis of CMOS two input NOR Gate.
9	Explain the working of MOS system under external Bias.
10	Write a short note on CPL (Complementary Pass-Transistor Logic). Explain its usefulness.
11	Explain CMOS Transmission Gate in Detail.
12	Draw and explain transistor level implementation of clocked NOR based SR latch circuit.
13	Explain Zipper CMOS Circuits.
14	Explain Concept of Regularity, Modularity and Locality.
15	Discuss Scan based Techniques for Testing.
16	Discuss Built-in Self Test (BIST) Techniques.
17	Discuss basic steps of Fabrication process flow.
18	Explain basic steps of LOCOS process. What is bird's beak region?
19	Explain major types of MOSFET capacitances and show its variations under different operating conditions and physical parameters
20	Explain CMOS D – Latch and edge triggered Flip-Flop.
	Implement following Boolean functions using CMOS Transmission Gate(TG): (i) F1 = AB + A'C' + AB'C (ii) F2 = AB + A'B'
21	Explain CMOS Transmission Gate in detail
22	Discuss NORA CMOS Logic
23	Discuss Scan Based Techniques for Testing.
24	Explain Voltage Bootstrapping.
25	Describe different Ad HOC testable design techniques.
26	Explain Channel Length Modulation.
27	Explain any one down scaling techniques for MOSFET. Which technique is preferable?
28	Explain fabrication process of nMOS transistor with diagram
29	Draw & explain the basic structure of FPGA. Explain functioning of logic cell using lookup table approach.

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30	Discuss Complementary pass transistor logic. Realize the XOR gate using CPL.
31	Explain the basic principle of Pass transistor circuits. Also Explain logic '1' transfer.
32	Discuss Built-in Self Test (BIST) Techniques
33	List the important concern for the IC packaging technology. Also Explain different packaging technologies.
34	Give comparison between FPGA and CPLD.
35	Briefly discuss semiconductor memories.
36	Differentiate Static RAM and Dynamic RAM.
37	Write short note on logic gate arrays.
38	Explain PLA based finite state machines.
39	Write short note on micro coded controllers.
40	Discuss differential amplifiers.